A MEMORY SYSTEM AND METHOD OF ACCESSING THEREOF

Abstract of the Disclosure

A memory system (200) has an array of addressable storage elements (210) arranged in a plurality of rows and a plurality of columns, and decoding circuitry (220, 230) coupled to the array of addressable storage elements (210). The decoding circuitry (220, 230), in response to decoding a first address, accesses a first storage element of a first row of the plurality of rows, and, in response to decoding a second address consecutive to the first address, accesses a second storage element of a second row of the plurality of rows. The second row of the plurality of rows is different from the first row of the plurality of rows. By implementing a memory system wherein consecutive addresses correspond to storage elements of different rows, read disturb stresses along a single row can be minimized.